TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT FULL CMOS STATIC RAM

DESCRIPTION

The TC55V400FT/TR is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 3.6V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 0.5μA standby current (at V_{DD}=3V, Ta=25°C, maximum) when chip enable ($\overline{CE1}$) is asserted high or (CE2) is asserted low. There are three control inputs. $\overline{CE1}$ and CE2 are used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. Data byte control pin ($\overline{LB}$, $\overline{UB}$) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of −40° to 85°C, the TC55V400FT/TR can be used in environments exhibiting extreme temperature conditions. The TC55V400FT/TR is available in normal and reverse pinout plastic 48-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
  Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.7 to 3.6V
- Power down features using $\overline{CE1}$ and CE2
- Data retention supply voltage of 1.5 to 3.6V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of −40° to 85°C
- Standby current (maximum)

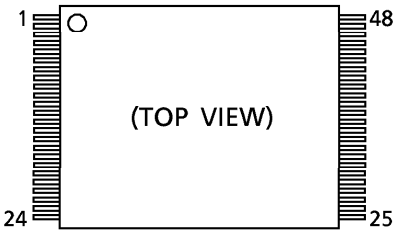
3.6V	7 μA
3.0V	5 μA

- Access Times (maximum):

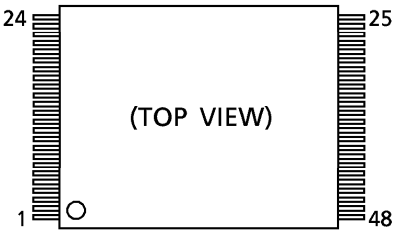
	TC55V400FT/TR		
	-70	-85	-10
Access Time	70 ns	85 ns	100 ns
$\overline{CE1}$ Access Time	70 ns	85 ns	100 ns
CE2 Access Time	70 ns	85 ns	100 ns
$\overline{OE}$ Access Time	35 ns	45 ns	50 ns

- Package:
  TSOP I 48-P-1214-0.50 (FT) (Weight:0.38g typ)
  TSOP I 48-P-1214-0.50A (TR) (Weight:0.38g typ)

PIN ASSIGNMENT (TOP VIEW)



(FT : Normal pinout)



(TR : Reverse pinout)

PIN NAMES

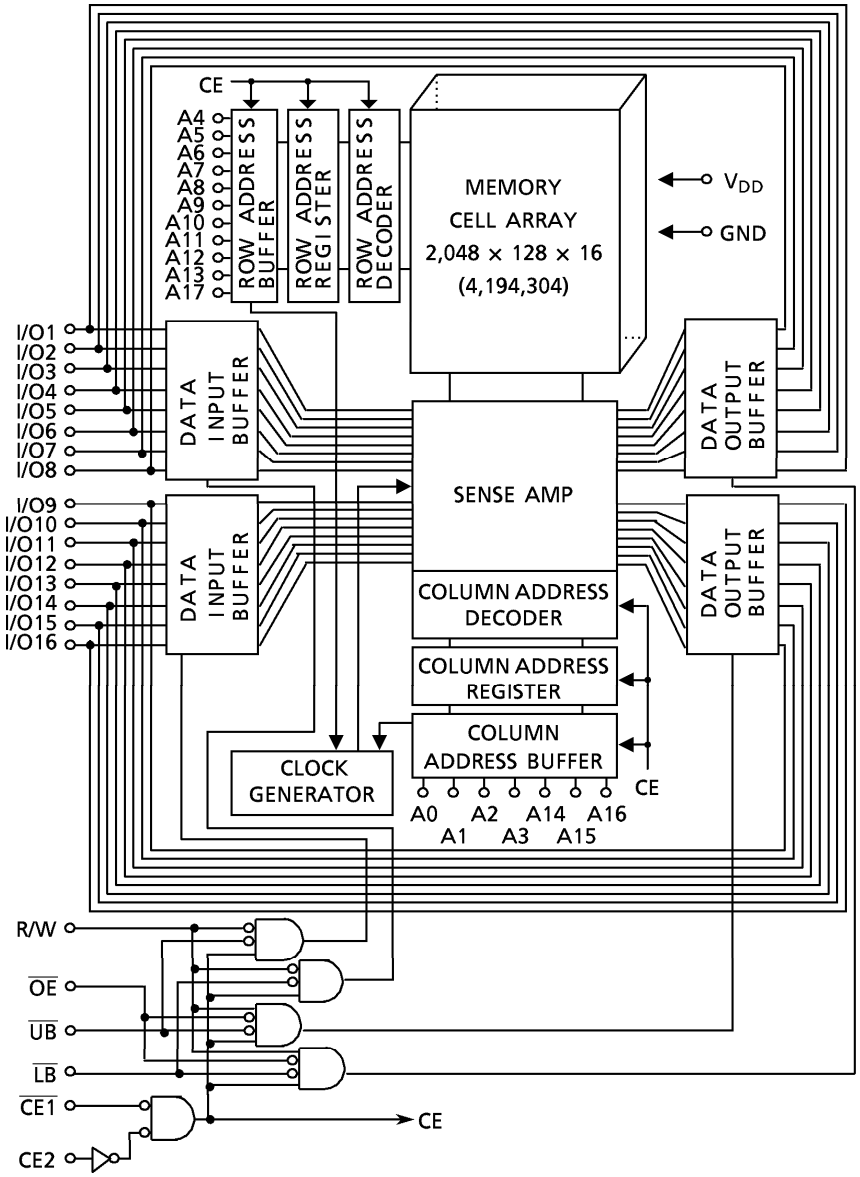
A0 to A17	Address Inputs
$\overline{CE1}$, CE2	Chip Enable Input
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
I/O1 to I/O16	Data Inputs / Outputs
V_{DD}	Power
GND	Ground
NC	No Connection

(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A15	A14	A13	A12	A11	A10	A9	A8	NC	NC	R/W	CE2	NC	$\overline{UB}$	$\overline{LB}$	NC
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A17	A7	A6	A5	A4	A3	A2	A1	A0	$\overline{CE1}$	GND	$\overline{OE}$	I/O1	I/O9	I/O2	I/O10
Pin No.	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Pin Name	I/O3	I/O11	I/O4	I/O12	V_{DD}	I/O5	I/O13	I/O6	I/O14	I/O7	I/O15	I/O8	I/O16	GND	NC	A16

980910EBA1

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	H	L	H	L	L	D_{OUT}	D_{OUT}	I_{DDO}
					H	L	High-Z	D_{OUT}	I_{DDO}
					L	H	D_{OUT}	High-Z	I_{DDO}
Write	L	H	×	L	L	L	D_{IN}	D_{IN}	I_{DDO}
					H	L	High-Z	D_{IN}	I_{DDO}
					L	H	D_{IN}	High-Z	I_{DDO}
Output Deselect	L	H	H	H	×	×	High-Z	High-Z	I_{DDO}
	L	H	×	×	H	H			
Standby	H	×	×	×	×	×	High-Z	High-Z	I_{DDS}
	×	L	×	×	×	×			

Note: × = don't care. H = logic high. L = logic low.

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	− 0.3 to 4.6	V
V_{IN}	Input Voltage	− 0.3 * to 4.6	V
$V_{I/O}$	Input/Output Voltage	− 0.5 to V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	− 55 to 150	°C
T_{opr}	Operating Temperature	− 40 to 85	°C

* − 3.0 V when measured at a pulse width of 30 ns.

DC RECOMMENDED OPERATING CONDITIONS (Ta = − 40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	2.7	−	3.6	V
V_{IH}	Input High Voltage	2.2	−	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	− 0.3 *	−	0.6	V
V_{DH}	Data Retention Supply Voltage	1.5	−	3.6	V

* − 3.0 V when measured at a pulse width of 30 ns.

DC CHARACTERISTICS (Ta = − 40° to 85°C, V_{DD} = 2.7 to 3.6V)

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}				−	−	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} − 0.5 V				− 0.5	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V				2.1	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 V to V_{DD}				−	−	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH} and I_{OUT} = 0 mA Other Input = V_{IH}/V_{IL}	V_{DD} = 3 V ± 10%	Tcycle = min	-70	−	−	50	mA
					-85,-10	−	−	45	
				Tcycle = 1 μs		−	−	10	
			V_{DD} = 3.3 V ± 0.3 V	Tcycle = min	-70	−	−	55	
					-85,-10	−	−	50	
				Tcycle = 1 μs		−	−	12	
I_{DDO2}		$\overline{CE1}$ = 0.2 V and CE2 = V_{DD} − 0.2 V and R/W = V_{DD} − 0.2 V, I_{OUT} = 0 mA Other Inputs = V_{DD} − 0.2V/0.2V	V_{DD} = 3 V ± 10%	Tcycle = min	-70	−	−	45	
					-85,-10	−	−	40	
				Tcycle = 1 μs		−	−	5	
			V_{DD} = 3.3 V ± 0.3 V	Tcycle = min	-70	−	−	50	
					-85,-10	−	−	45	
				Tcycle = 1 μs		−	−	6	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}				−	−	2	mA
I_{DDS2} (Note)		$\overline{CE1}$ = V_{DD} − 0.2 V or CE2 = 0.2 V V_{DD} = 1.5 to 3.6 V	V_{DD} = 3 V ± 10%	Ta = 25°C		−	−	0.6	μA
				Ta = − 40 to 85°C		−	−	6	
			V_{DD} = 3.3 V ± 0.3 V	Ta = 25°C		−	−	0.7	
				Ta = − 40 to 85°C		−	−	7	
			V_{DD} = 3 V	Ta = 25°C		−	0.05	0.5	
				Ta = − 40 to 40°C		−	−	1	
				Ta = − 40 to 85°C		−	−	5	

Note: In standby mode with $\overline{CE1} \geqq V_{DD} - 0.2V$, these limits are assured for the condition CE2 $\geqq V_{DD} - 0.2V$ or CE2 $\leqq$ 0.2V.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = – 40° to 85°C, V_{DD} = 2.7 to 3.6V)

READ CYCLE

SYMBOL	PARAMETER	TC55V400FT/TR						UNIT
		-70		-85		-10		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	70	–	85	–	100	–	ns
t_{ACC}	Address Access Time	–	70	–	85	–	100	
t_{CO1}	Chip Enable ($\overline{CE1}$) Access Time	–	70	–	85	–	100	
t_{CO2}	Chip Enable (CE2) Access Time	–	70	–	85	–	100	
t_{OE}	Output Enable Access Time	–	35	–	45	–	50	
t_{BA}	Data Byte Control Access Time	–	35	–	45	–	50	
t_{COE}	Chip Enable Low to Output Active	5	–	5	–	5	–	
t_{OEE}	Output Enable Low to Output Active	0	–	0	–	0	–	
t_{BE}	Data Byte Control Low to Output Active	0	–	0	–	0	–	
t_{OD}	Chip Enable High to Output High-Z	–	30	–	35	–	40	
t_{ODO}	Output Enable High to Output High-Z	–	30	–	35	–	40	
t_{BD}	Data Byte Control High to Output High-Z	–	30	–	35	–	40	
t_{OH}	Output Data Hold Time	10	–	10	–	10	–	

WRITE CYCLE

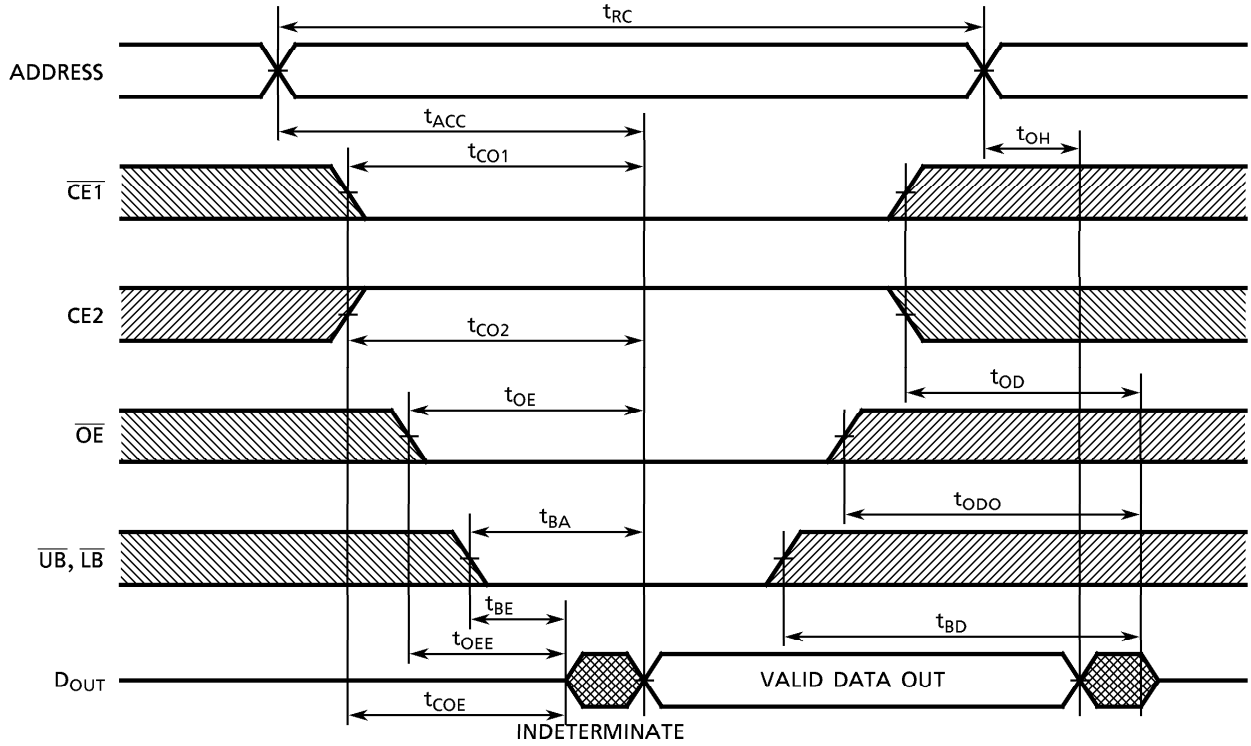
SYMBOL	PARAMETER	TC55V400FT/TR						UNIT
		-70		-85		-10		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	70	–	85	–	100	–	ns
t_{WP}	Write Pulse Width	50	–	55	–	60	–	
t_{CW}	Chip Enable to End of Write	60	–	70	–	80	–	
t_{BW}	Data Byte Control to End of Write	50	–	55	–	60	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{ODW}	R/W Low to Output High-Z	–	30	–	35	–	40	
t_{OEW}	R/W High to Output Active	0	–	0	–	0	–	
t_{DS}	Data Setup Time	30	–	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

AC TEST CONDITIONS

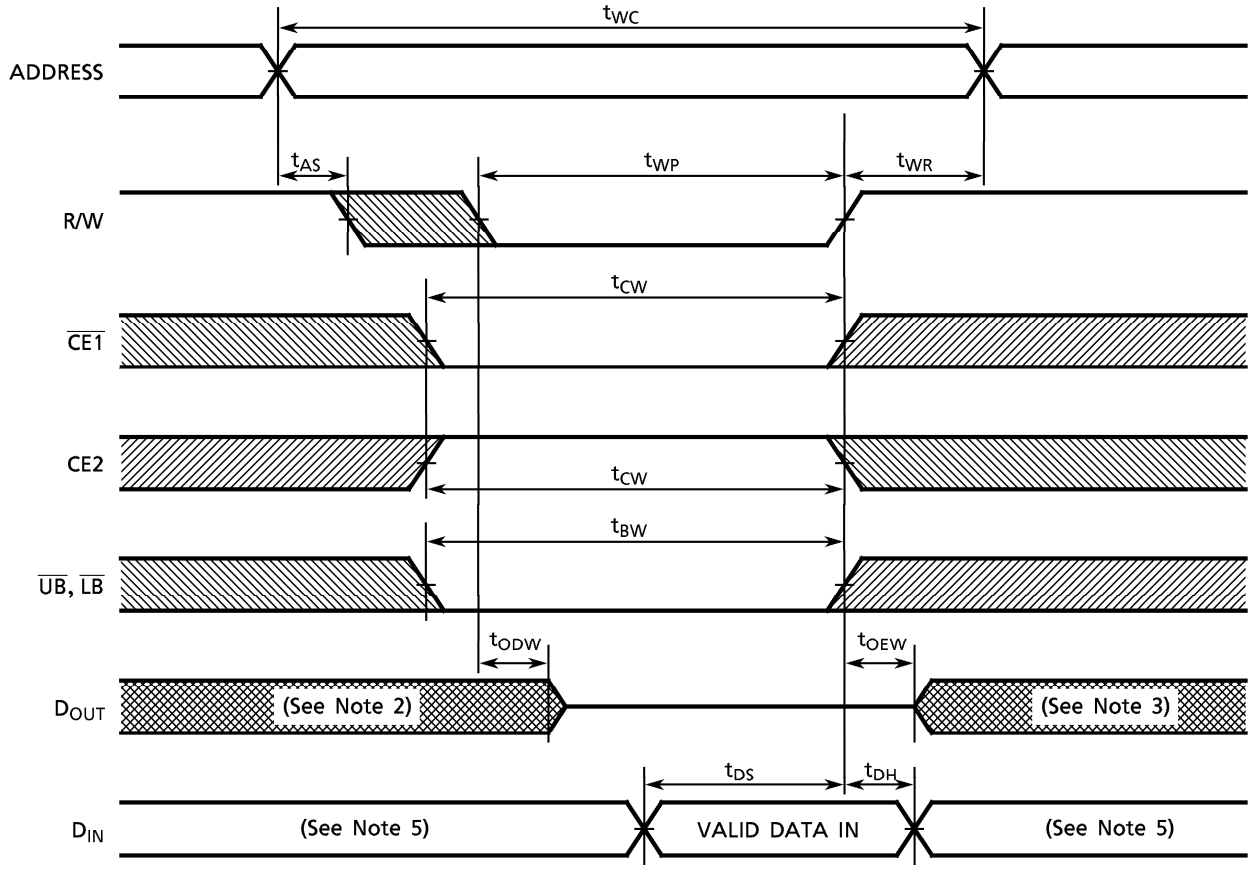
Output load: 30 pF + one TTL gate (-70)
: 100 pF + one TTL gate (-85, -10)
Input pulse level: 0.4 V, 2.4 V
Timing measurements: 1.5 V
Reference level: $V_{DD} \times 0.5$
t_R, t_F: 5 ns

TIMING DIAGRAMS

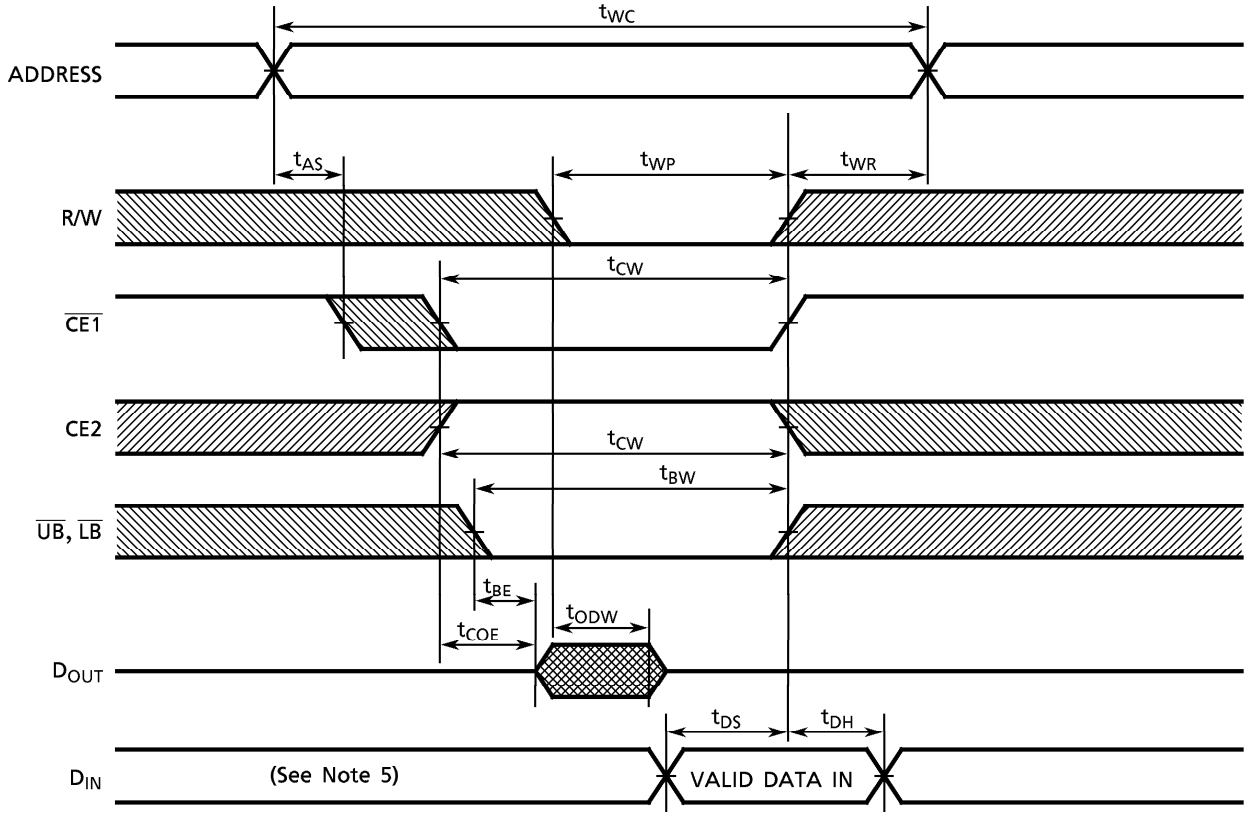
READ CYCLE (See Note 1)



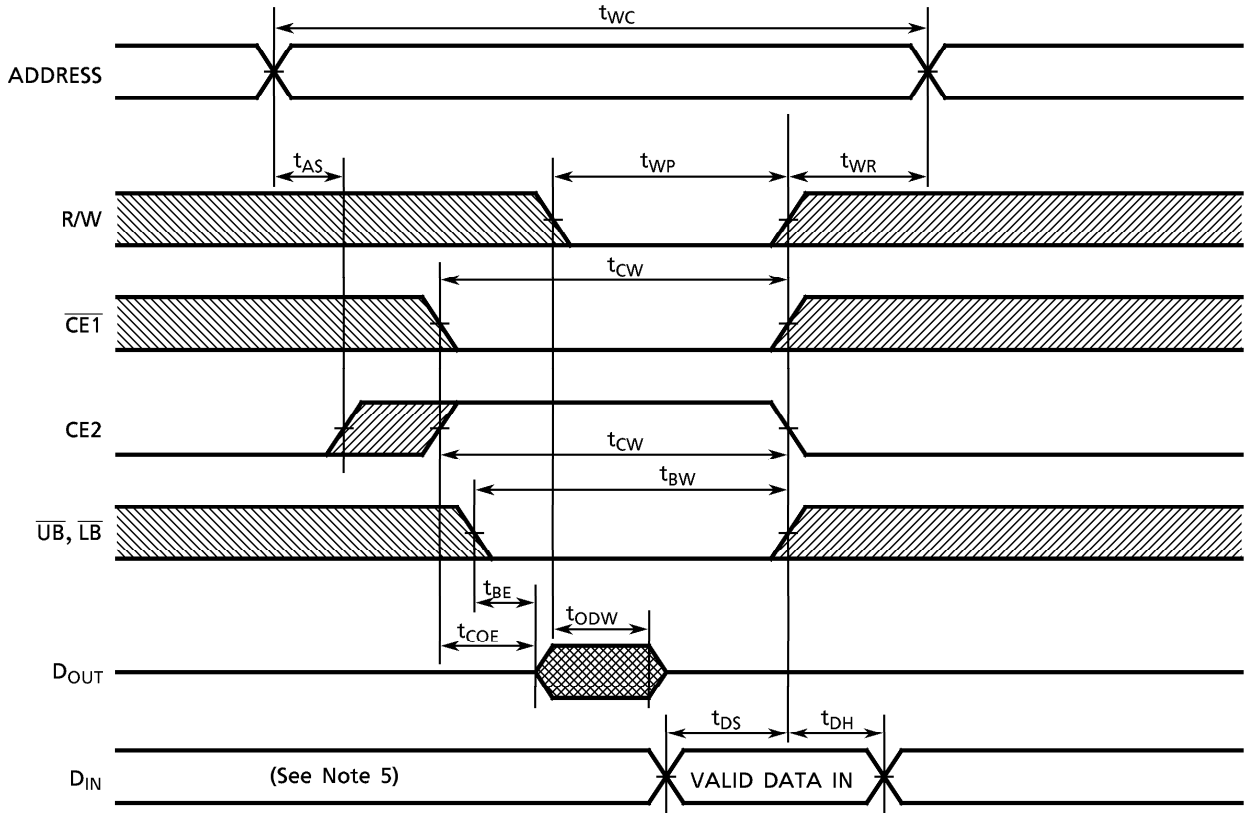
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



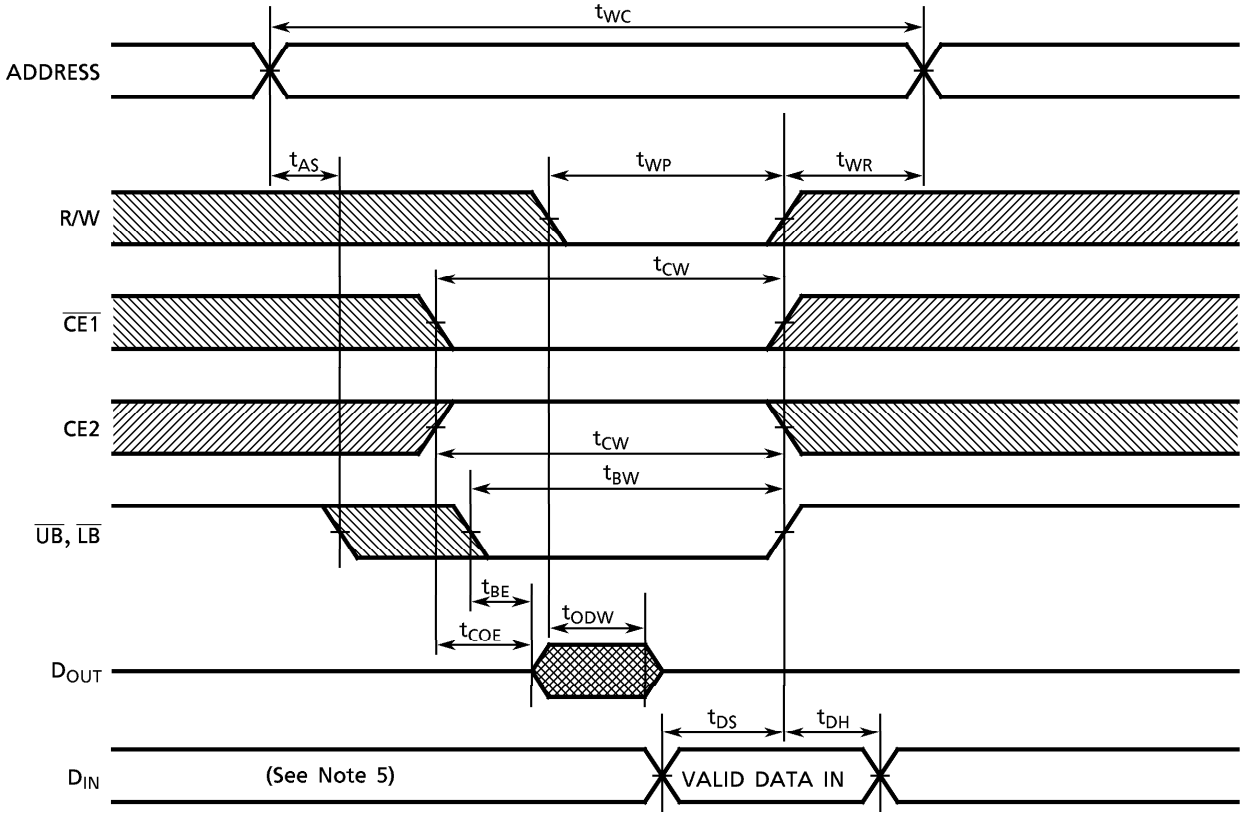
WRITE CYCLE 2 ($\overline{CE1}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)



WRITE CYCLE 4 ($\overline{UB}$, $\overline{LB}$ CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE1}$ goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE1}$ goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

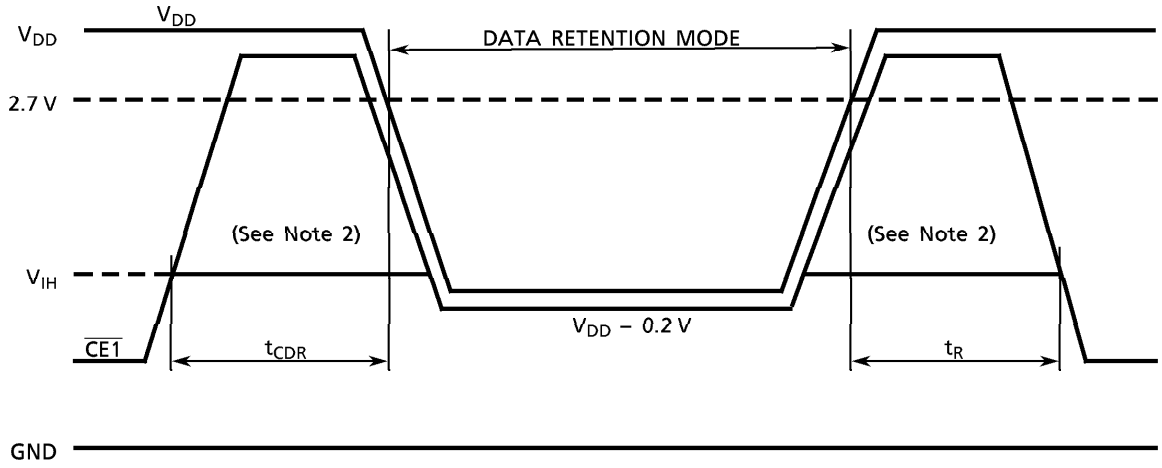
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = −40° to 85°C)

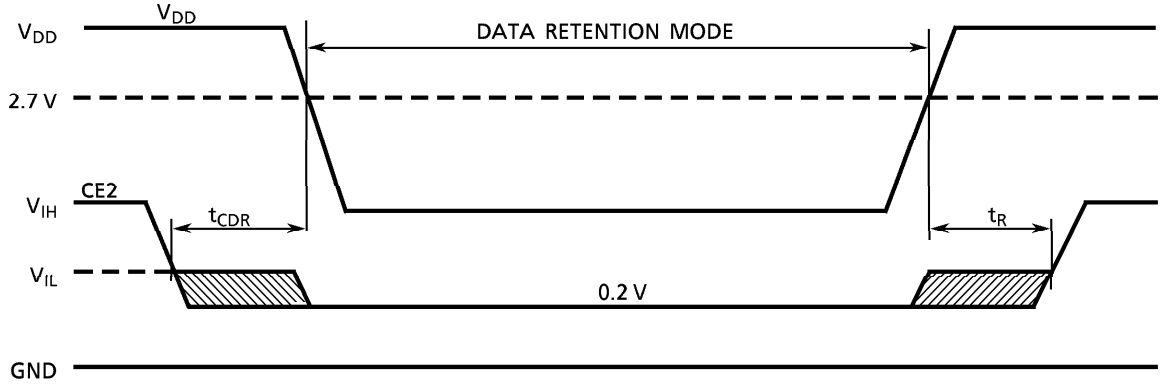
SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage			1.5	–	3.6	V
I_{DDS2}	Standby Current	V_{DH} = 3.0 V	Ta = −40° to 40°C	–	–	1	μA
			Ta = −40° to 85°C	–	–	5	
		V_{DH} = 3.6 V	Ta = −40° to 85°C	–	–	7	
t_{CDR}	Chip Deselect to Data Retention Mode Time			0	–	–	nS
t_R	Recovery Time			t_{RC} (See Note)	–	–	nS

Note: Read cycle time

$\overline{CE1}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



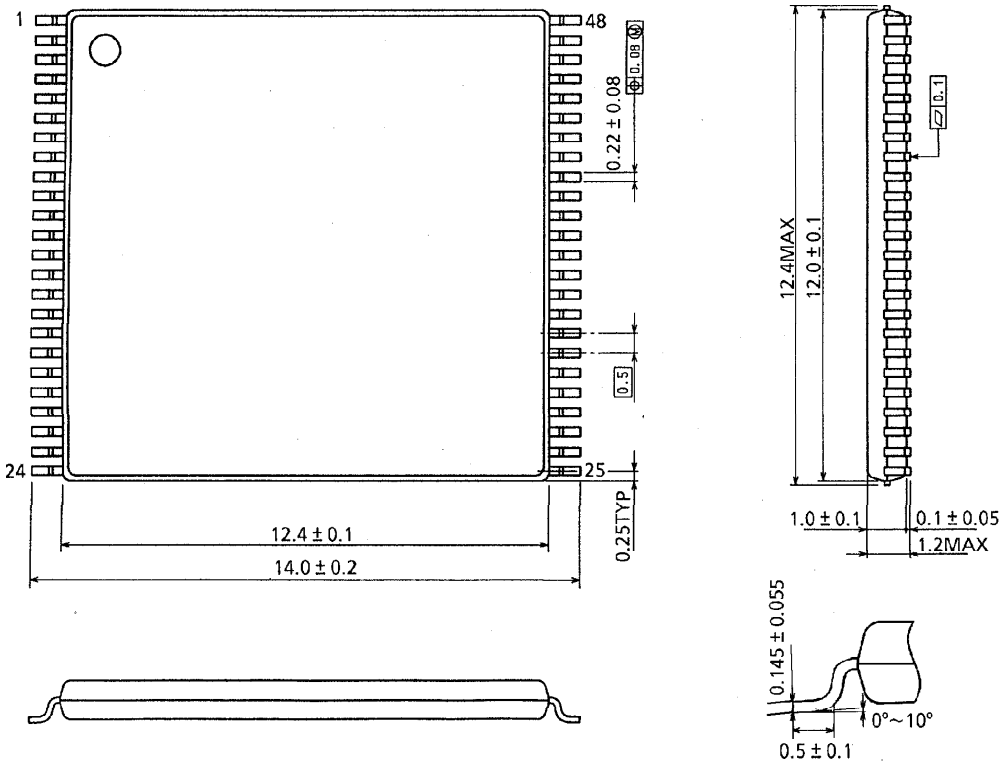
Note: (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is entered when CE2 ≦ 0.2 V or CE2 ≧ V_{DD} − 0.2 V.

(2) When $\overline{CE1}$ is operating at the V_{IH} level (2.2 V), the operating current is given by I_{DDS1} during the transition of V_{DD} from 3.6 to 2.4 V.

(3) In CE2 controlled data retention mode, minimum standby current mode is entered when CE2 ≦ 0.2 V.

PACKAGE DIMENSIONS (TSOP I 48-P-1214-0.50)

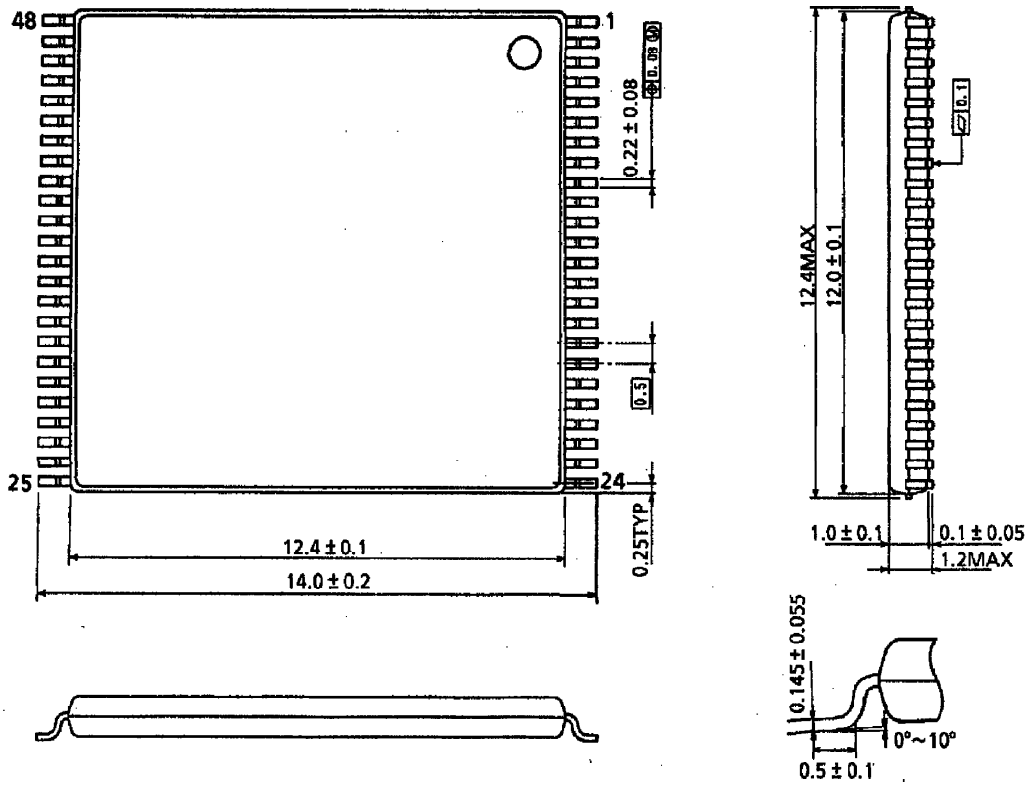
Units in mm



Weight: 0.38 g (typ)

PACKAGE DIMENSIONS (TSOP I 48-P-1214-0.5A)

Units in mm



Weight: 0.38 g (typ)