TC74HC298AP/AF

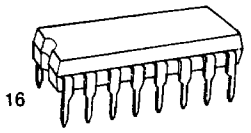
QUAD 2-CHANNEL MULTIPLEXER WITH OUTPUT REGISTER

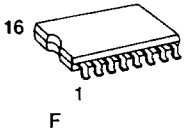
The TC74HC298A is a high speed CMOS 2-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It contains a 4-bit 2-channel multiplexer and a 4-bit output register.When the word select input(W.S)is held low,the data of word 1(A1,B1,C1,D1)is selected and is applied to the registers.When W.S. is held high,the data of word 2(A2,B2,C2,D2)will be applied to the registers. This selected data is transfered to the output(QA,QB, QC, QD) on the negative going transition of $\overline{CLOCK}$.

All inputs are equipped with protection circuits against static dischage or transient excess voltage.

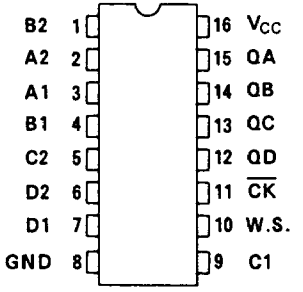




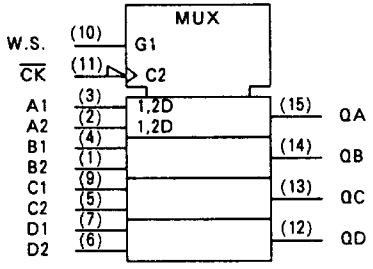
FEATURES:

- High Speed ····· f_{MAX}=73MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS298

PIN ASSIGNMENT



IEC LOGIC SYMBOL

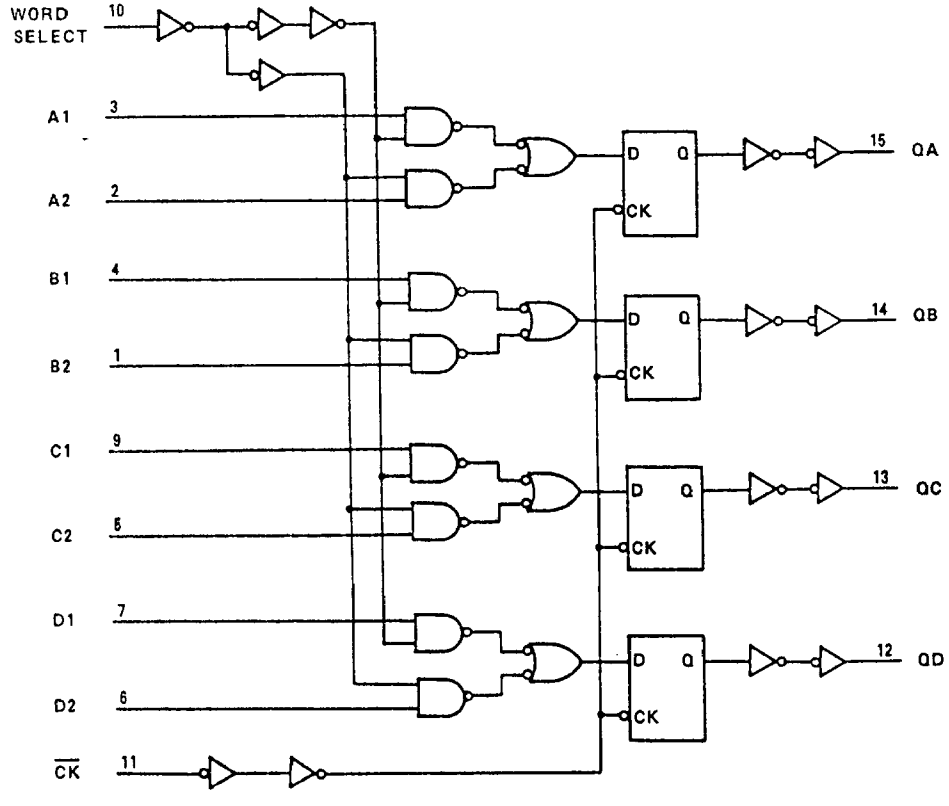


TRUTH TABLE

INPUTS		OUTPUTS			
WORD SELECT	$\overline{CK}$	QA	QB	QC	QD
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	↑	QA0	QB0	QD0	QD0

X : Don't care (Including transition)
a1, a2····· : The Level of steady-state Input at A1, A2, etc
QA0, QB0··· : The level of QA, QB, etc. entered on the most recent negative transition of the clock input.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{CK}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (A, B, C, D)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set−up Time (W. S.)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (A, B, C, D)	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Minimum Hold Time (W. S.)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Clock Frequency	f		2.0	−	7	6	MHz
			4.5	−	35	27	
			6.0	−	41	33	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CK}$−Q)	t_{pLH} t_{pHL}		−	12	21	
Maximum Clock Frequency	f_{MAX}		38	73	−	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CK}$−Q)	t_{pLH} t_{pHL}		2.0	−	45	125	−	155	
			4.5	−	15	25	−	31	
			6.0	−	13	21	−	26	
Maximum Clock Frequency	f_{MAX}		2.0	7	22	−	6	−	
			4.5	35	67	−	28	−	
			6.0	41	79	−	33	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	39	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per bit)}$$

And the total C_{PD} when n−bits operate can be gained by the following equation:

$$C_{PD}\text{ (total)}=27+12 \cdot n$$