TC74HC356AP/AF

8-CHANNEL MULTIPLEXER WITH INPUT REGISTER

The TC74HC356A is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device contains an 8 channel digital multiplexer with an 8-bit input data register(D0~D7), a 3-bit address input register(S0~S2)and 3-state outputs.

Data from one of the eight inputs will be shifted onto the Y output (non-inverted)and the W output (inverted) pins as determined by the address data.

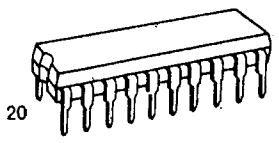
Its outputs go into a high-impedance state when either $\overline{G1}$ or $\overline{G2}$ is held high or G3 is held low.

In the TC74HC356A, the data is stored into the 8-bit flip-flop at the positive going transition of the clock input (CLOCK).

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=25ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS356



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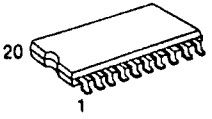

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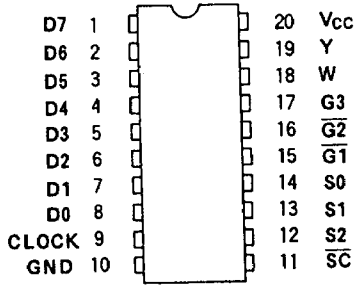
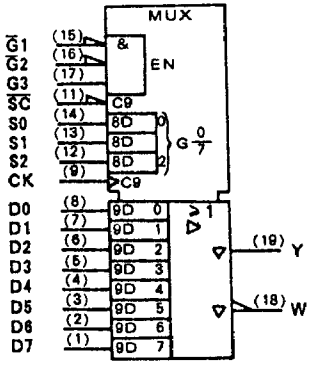
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

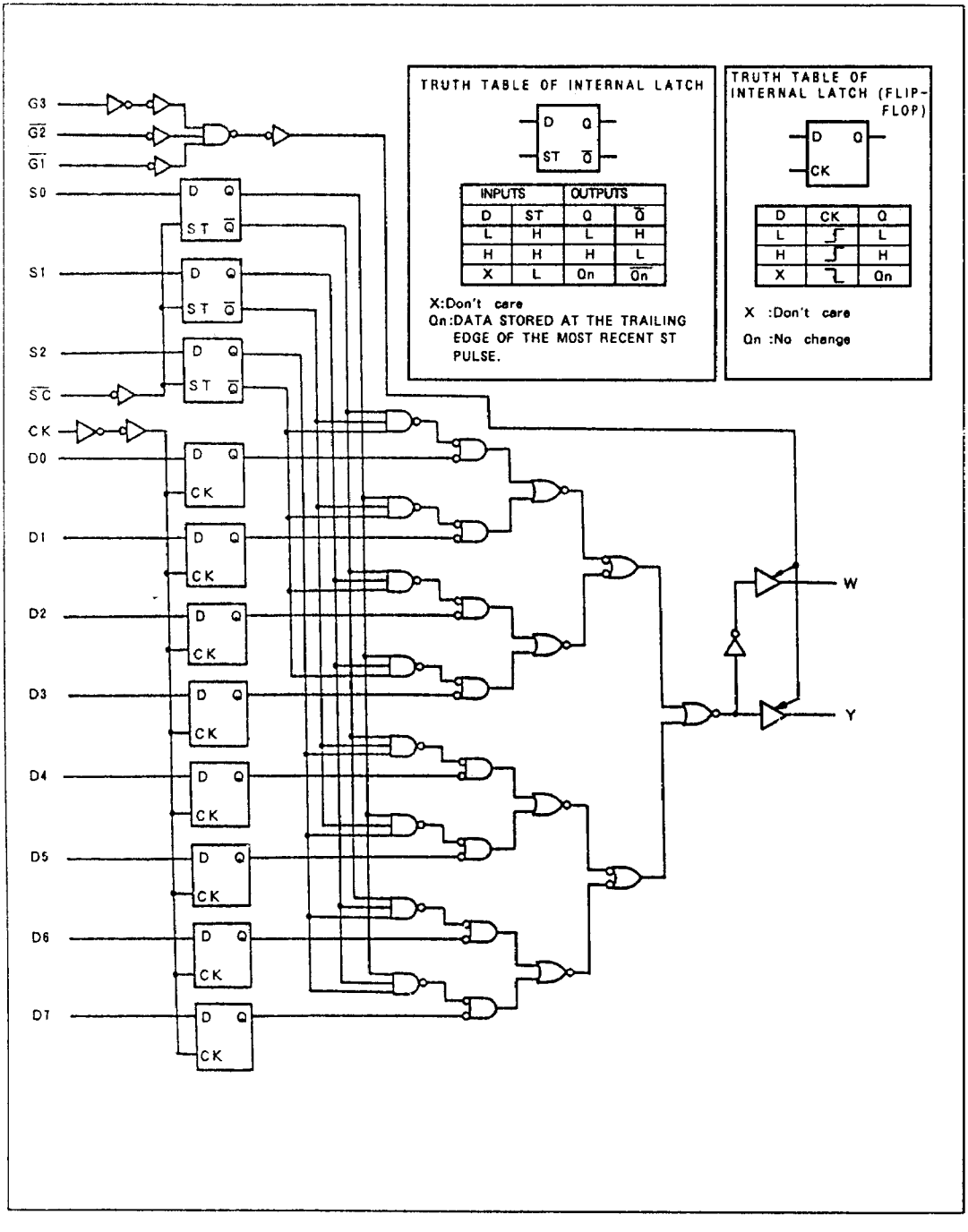
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT #			CLOCK	OUTPUT ENABLES			W	Y
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3		
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	↓	L	L	H	$\overline{D0n}$	D0n
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	↓	L	L	H	$\overline{D1n}$	D1n
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	↓	L	L	H	$\overline{D2n}$	D2n
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	↓	L	L	H	$\overline{D3n}$	D3n
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	↓	L	L	H	$\overline{D4n}$	D4n
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	↓	L	L	H	$\overline{D5n}$	D5n
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	↓	L	L	H	$\overline{D6n}$	D6n
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	↓	L	L	H	$\overline{D7n}$	D7n

X:Don't care
Z:High Impedance
D0n·····D7:The level of steady-state inputs at inputs D0 through D7, respectively, before the most recent "L" to "H" transition of data control.
#:This column shows the input address setup with $\overline{SC}$ low.

SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃		Ta=−40∼85℃	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SC}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time (Dn)	t_S		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set-up Time (Sn)	t_S		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (Dn)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Hold Time (Sn)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	24	
			6.0	−	36	28	

AC ELECTRICAL CHARCTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	11	−	13	
Propagation Delay Time (CLOCK−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	99	240	−	300	
				4.5	−	28	48	−	60	
				6.0	−	22	41	−	51	
			150	2.0	−	117	280	−	350	
				4.5	−	33	56	−	70	
				6.0	−	26	48	−	60	
Propagation Delay Time (Sn−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	111	260	−	325	
				4.5	−	32	52	−	65	
				6.0	−	24	44	−	55	
			150	2.0	−	128	300	−	375	
				4.5	−	37	60	−	75	
				6.0	−	28	51	−	64	
Propagation Delay Time ($\overline{SC}$−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	115	270	−	340	
				4.5	−	33	54	−	68	
				6.0	−	25	46	−	58	
			150	2.0	−	132	310	−	390	
				4.5	−	38	62	−	78	
				6.0	−	29	53	−	66	
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	50	2.0	−	48	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	11	21	−	26	
			150	2.0	−	65	165	−	205	
				4.5	−	19	33	−	41	
				6.0	−	15	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	50	2.0	−	43	155	−	195	
				4.5	−	18	31	−	39	
				6.0	−	16	26	−	33	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	20	−	5	−	
				4.5	31	80	−	24	−	
				6.0	36	32	−	28	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	$C_{PD(1)}$				−	59	−	−	−	

Note(1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(op)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$