TC74HCT646AP
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OCTAL BUS TRANSCEIVER/REGISTER
TC74HCT646AP NON-INVERTING
TC74HCT648AP INVERTING

The TC74HCT646A/HCT648A are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

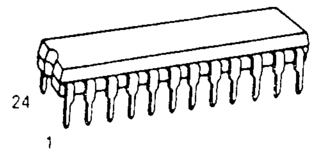
These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

The TC74HCT646A is a non-inverting output type while the TC74HCT648A is of the inverting output type.

All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed .... f_{MAX}=60MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation .... I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL Output .... V_{IH}=2V(Min.)V_{IL}=0.8V(Max.)
- Output Drive Capability .... 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ······ $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS646/648



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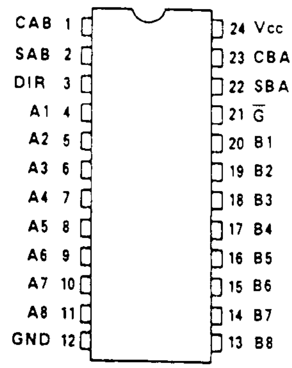
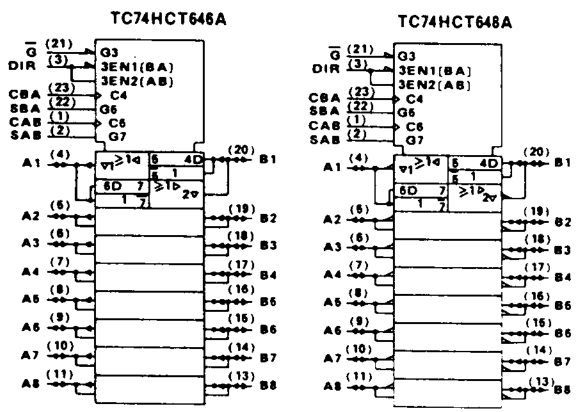
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

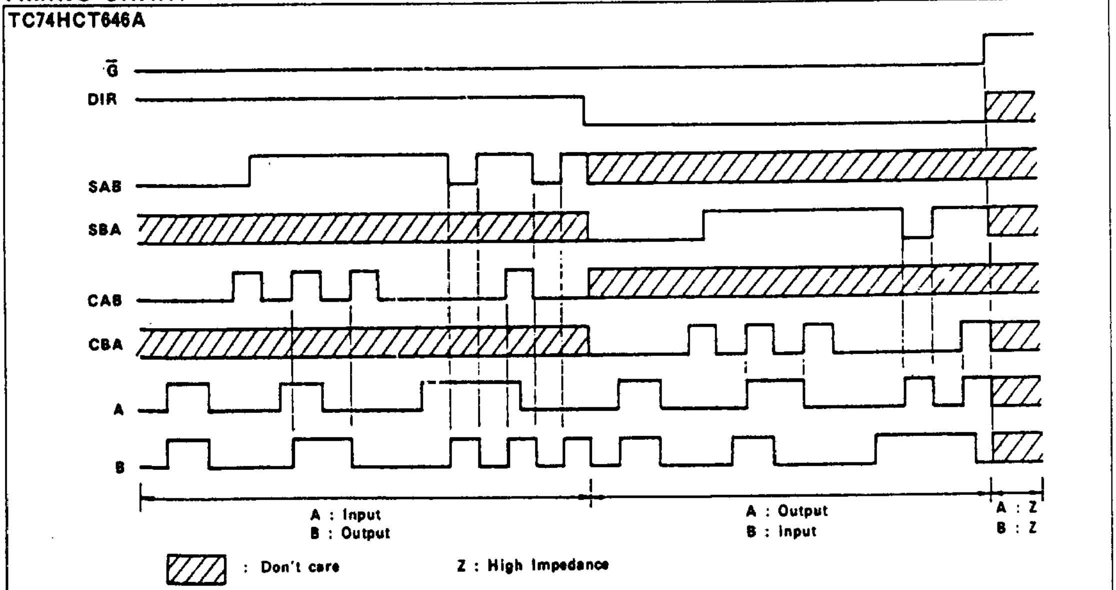
TRUTH TABLE

TC74HCT646A(The truth table for TC74HCT648A is the same, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X*	X*	X	X	INPUTS Z	INPUTS Z	The output funcions of A and B Busses are disabled.
		↑	↑	X	X	X	X	Both A and B Busses are used as inputs to the internal flips-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus
		↑	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↑	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↑	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↑	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

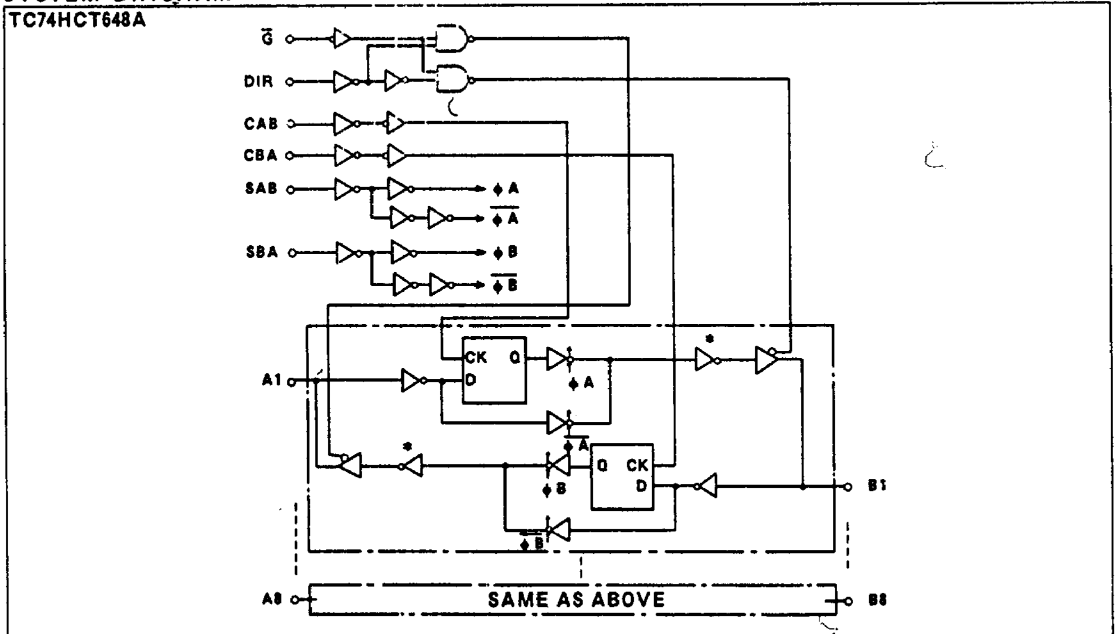
Notes :
- X : Don't Care
- Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs
- Z : High Impedance
- * The clock are not internally gated with either $\overline{G}$ or DIR. Therfore, data on the A and /or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART



Note: The timing chart for TC74HCT648A is the same, but with the outputs inverted.

SYSTEM DIAGRAM



Note: In case of TC74HCT646A output inverter marked * at A bus and B bus are eliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	Topr	−40~85	℃
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$I_{OH}=-20\,\mu A$	4.5	4.4	4.5	−	4.4	−	V
			$I_{OH}=-6\,\mu A$	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	$I_{OL}=20\,\mu A$	4.5	−	0.0	0.1	−	0.1	V
			$I_{OL}=6\,\mu A$	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{IN}=V_{CC}$ or GND		5.5	−	−	±0.5	−	±5.0	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	−	−	4.0	−	40.0	
	ΔI_{CC}	Per input: V_{IN}=0.5V or 2.4V Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		4.5 5.5	– –	15 14	19 17	ns
Minimum Set-up Time	t_s		4.5 5.5	– –	10 9	13 12	ns
Minimum Hold Time	t_h		4.5 5.5	– –	5 5	5 5	ns
Clock Frequency	f		4.5 5.5	– –	31 37	25 30	MHz

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	4.5 5.5	– –	7 6	12 11	– –	15 14	ns
Propagation Delay Time (BUS-BUS)	t_{pLH} t_{pHL}		50	4.5 5.5	– –	20 17	30 27	– –	38 34	ns
			150	4.5 5.5	– –	25 22	38 34	– –	48 43	ns
Propagation Delay Time (CAB, CBA-BUS)	t_{pLH} t_{pHL}		50	4.5 5.5	– –	29 26	44 40	– –	55 50	ns
			150	4.5 5.5	– –	34 31	52 47	– –	65 59	ns
Propagation Delay Time (SAB, SBA-BUS)	t_{pLH} t_{pHL}		50	4.5 5.5	– –	24 21	34 31	– –	43 39	ns
			150	4.5 5.5	– –	29 26	42 38	– –	53 46	ns
Output Enable time (DIR, $\overline{G}$-BUS)	t_{pZL} t_{pZH}	$R_L = 1\,k\Omega$	50	4.5 5.5	– –	26 23	38 34	– –	48 43	ns
			150	4.5 5.5	– –	31 28	46 41	– –	58 52	ns
Output Enable time (DIR, $\overline{G}$-BUS)	t_{pLZ} t_{pHZ}	$R_L = 1\,k\Omega$	50	4.5 5.5	– –	26 23	35 32	– –	44 40	ns
Maximum Clock Frequency	f_{MAX}		50	4.5 5.5	31 37	55 61	– –	25 30	– –	MHz
Input Capacitance	C_{IN}	DIR, $\overline{G}$, SAB, SBA, CAB, CBA			–	5	10	–	10	pF
Output Capacitance	C_{OUT}	An, Bn			–	13	–	–	–	pF
Power Dissipation Capacitance	$C_{PD}(1)$	TC74HCT646A			–	40	–	–	–	pF
		TC74HCT648A			–	39	–	–	–	pF

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$