

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74HCT652AP

## OCTAL BUS TRANSCEIVER / REGISTER (3-STATE)

The TC74HCT652A is high speed CMOS OCTAL BUS TRANSCEIVER / REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

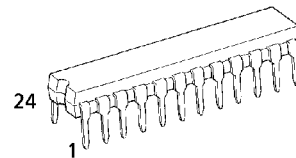
Its inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

ALL inputs are equipped with protection circuits against static discharge or transient excess voltage.

### FEATURES :

- High Speed.....  $f_{MAX} = 60 \text{ MHz (typ.)}$   
at  $V_{CC} = 5V$
- Low Power Dissipation.....  $I_{CC} = 4\mu\text{A (Max.)}$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL Output.....  $V_{IH} = 2.0V \text{ (Min.)}$   
 $V_{IL} = 0.8V \text{ (Max.)}$
- Output Drive Capability..... 15 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 6\text{mA (Min.)}$
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74LS652



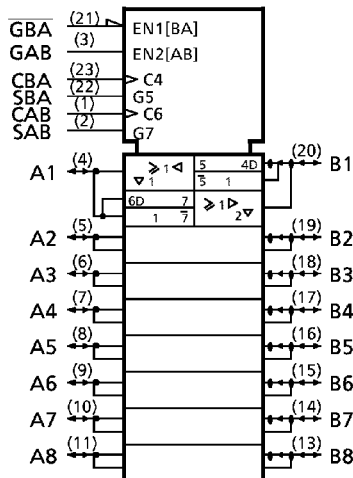
P (DIP24-P-300-2.54)  
Weight : 1.50g (Typ.)

### PIN ASSIGNMENT

CAB	1	24	V <sub>CC</sub>
SAB	2	23	CBA
GAB	3	22	SBA
A1	4	21	GBA
A2	5	20	B1
A3	6	19	B2
A4	7	18	B3
A5	8	17	B4
A6	9	16	B5
A7	10	15	B6
A8	11	14	B7
GND	12	13	B8

(TOP VIEW)

### IEC LOGIC SYMBOL









### APPLICATION NOTES

- 1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

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TRUTH TABLE

GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA	A	B	Function
L	H	X*	X*	X	X	INPUTS Z	INPUTS Z	The output functions of A and B Busses are disabled.
				X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
H	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
			X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
			X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*		X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*		X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
H	L	X*	X*	H	H	OUTPUTS Qn	OUTPUTS Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.

Notes : X : Don't Care

Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

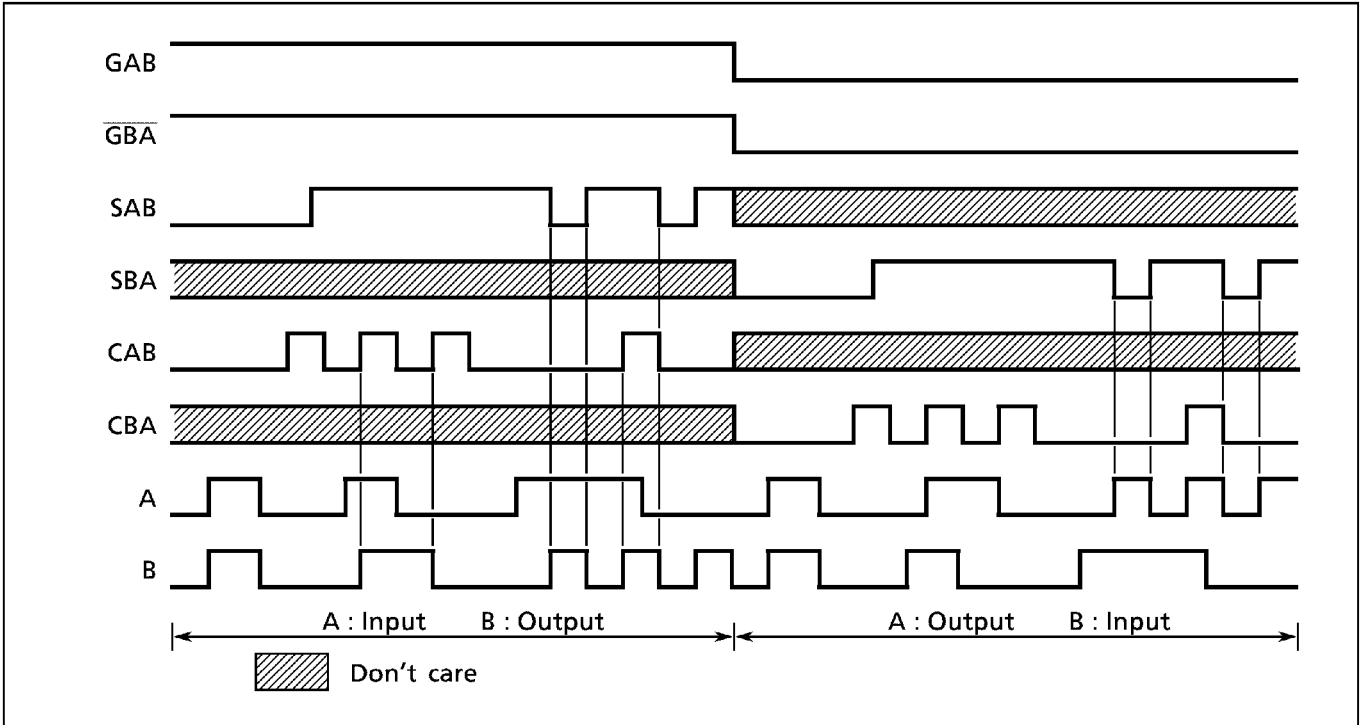
Z : High Impedance

\* : The clock are not internally gated with either GAB or  $\overline{\text{GBA}}$ . Therefore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

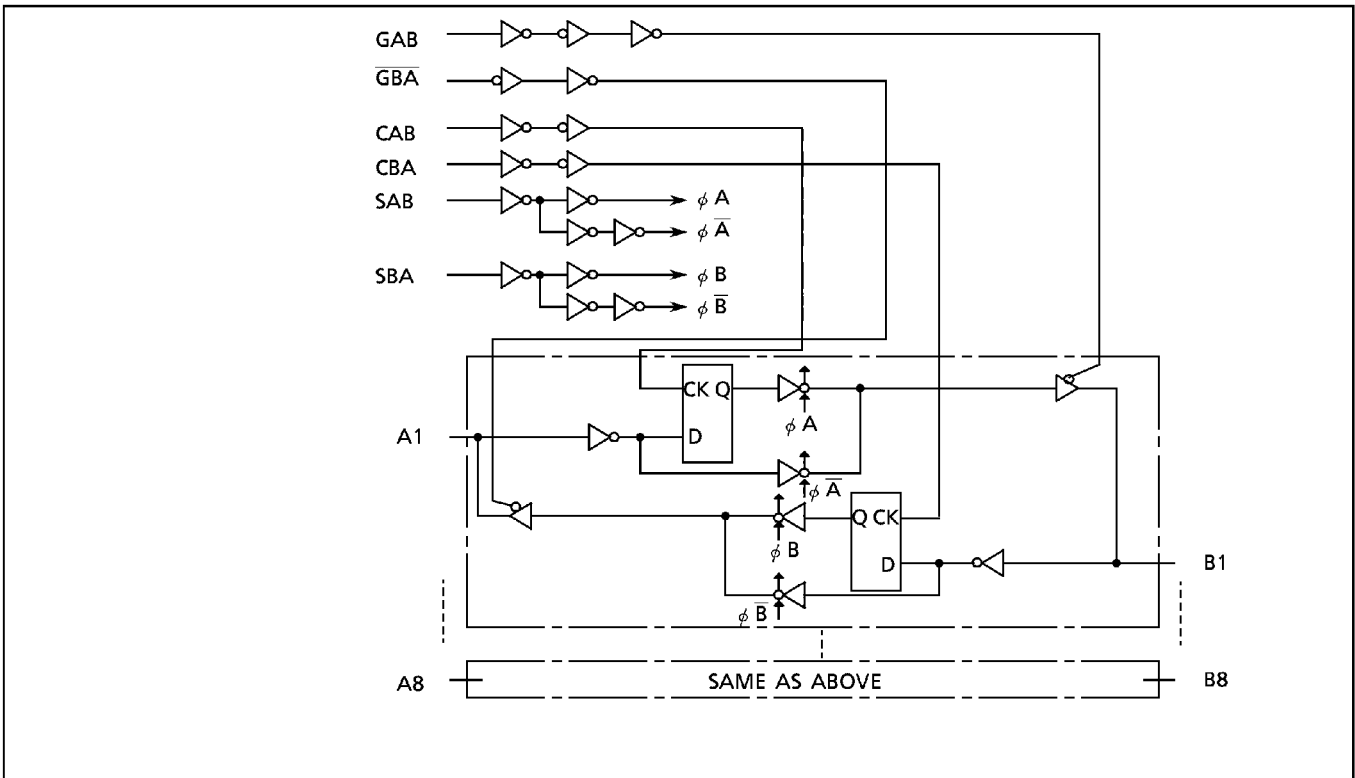
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TIMING CHART



SYSTEM DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	±20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±35	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±75	mA
Power Dissipation	$P_D$	500 (DIP)*	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  should be applied up to 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~500	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	$V_{IH}$		4.5 } 5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	$V_{IL}$		4.5 } 5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -6 \text{ mA}$	4.5	4.18	4.31	—	4.13	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 6 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
3 - State Output Off - State Current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5	—	—	±0.5	—	±5.0	$\mu\text{A}$	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	±0.1	—	±1.0	$\mu\text{A}$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	$\mu\text{A}$	
	$I_C$	Per input: $V_{IN} = 0.5\text{V}$ or $2.4\text{V}$ Other input: $V_{CC}$ or GND	5.5	—	—	2.0	—	2.9	mA	

TIMING REQUIREMENTS (Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C	UNIT
			V <sub>CC</sub> (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$		4.5	—	15	19	ns
	$t_{W(H)}$		5.5	—	14	17	
Minimum Set-up Time	$t_s$		4.5	—	10	13	
			5.5	—	9	12	
Minimum Hold Time	$t_h$		4.5	—	5	5	
			5.5	—	5	5	
Clock Frequency	f		4.5	—	31	25	MHz
			5.5	—	37	30	

AC ELECTRICAL CHARACTERISTICS ( Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	CL		Ta = 25°C			Ta = -40~85°C		UNIT
			(pF)	V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	$t_{TLH}$		50	4.5	—	7	12	—	15	ns
	$t_{THL}$			5.5	—	6	11	—	14	
Propagation Delay Time (BUS—BUS)	$t_{pLH}$		50	4.5	—	20	30	—	38	
				5.5	—	17	27	—	34	
	$t_{pHL}$		150	4.5	—	25	38	—	48	
				5.5	—	22	34	—	43	
Propagation Delay Time (CAB, CBA—BUS)	$t_{pLH}$		50	4.5	—	29	44	—	55	
				5.5	—	26	40	—	50	
	$t_{pHL}$		150	4.5	—	34	52	—	65	
				5.5	—	31	47	—	59	
Propagation Delay Time (SAB, SBA—BUS)	$t_{pLH}$		50	4.5	—	24	34	—	43	
				5.5	—	21	31	—	39	
	$t_{pHL}$		150	4.5	—	29	42	—	53	
				5.5	—	26	38	—	48	
Output Enable Time (GAB, $\overline{\text{GBA}}$ —BUS)	$t_{pZL}$	$R_L = 1\text{k}\Omega$	50	4.5	—	22	33	—	41	
				5.5	—	20	30	—	37	
	$t_{pZH}$		4.5	—	27	41	—	51		
			5.5	—	24	37	—	46		
Output Enable Time (GAB, $\overline{\text{GBA}}$ —BUS)	$t_{pLZ}$	$R_L = 1\text{k}\Omega$	50	4.5	—	24	35	—	44	
				5.5	—	22	32	—	40	
$t_{pHZ}$	4.5		—	24	35	—	44			
	5.5		—	22	32	—	40			
Maximum Clock Frequency	f <sub>MAX</sub>		50	4.5	31	55	—	25	MHz	
				5.5	37	61	—	30		
Input Capacitance	C <sub>IN</sub>	GAB, $\overline{\text{GBA}}$ , SAB, SBA, CAB, CBA			—	5	10	—	10	pF
Output Capacitance	C <sub>OUT</sub>	An, Bn			—	13	—	—	—	
Power Dissipation Capacitance	C <sub>PD</sub> (1)				—	39	—	—	—	

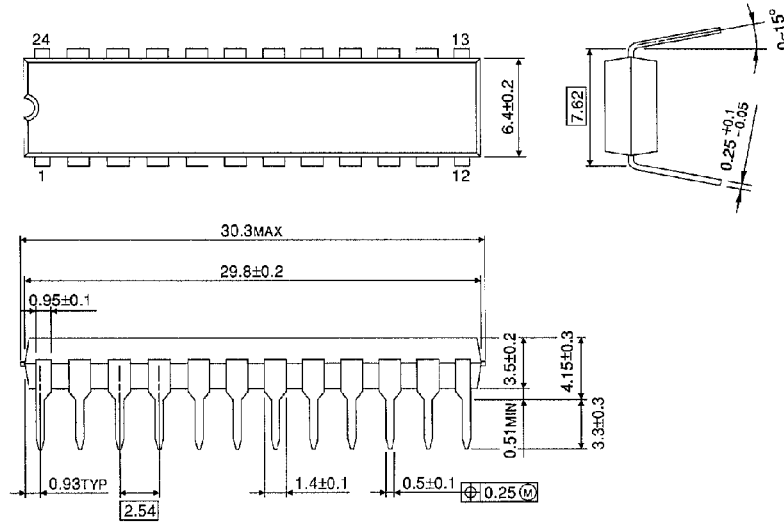
Note(1): C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

DIP 24PIN OUTLINE DRAWING (DIP24-P-300-2.54)

Unit in mm



Weight : 1.50g (Typ.)